

Radiation-Resilient Volatile Memory for Satellite Systems: A Review of Fault-Aware Design Techniques for SRAM and DRAM

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The escalating complexity of modern satellite missions ranging from high-resolution Earth observation to deep-space exploration has driven a transition from specialized radiation-hardened-by-process components toward high-density Commercial-Off-The-Shelf (COTS) volatile memories. While Static Random-Access Memory (SRAM) and Dynamic Random-Access Memory (DRAM) offer the high-speed data processing required for these applications, they remain critically susceptible to the harsh extra-terrestrial radiation environment. This environment is characterized by Total Ionizing Dose (TID) effects and Single Event Effects (SEE), which induce "soft errors" that can compromise mission integrity or lead to catastrophic system failure.

This review paper provides a comprehensive analysis of state-of-the-art Fault-Aware Design Techniques and Radiation Hardening by Design (RHBD) strategies specifically engineered for satellite-based volatile memory. As CMOS technology scales into the deep-submicron and nanoscale regimes (below 28nm), the critical charge of memory nodes decreases significantly, facilitating not only Single Event Upsets (SEU) but also increasingly prevalent Single Event Multiple-Node Upsets (SEMNU). We perform a detailed evaluation of advanced SRAM cell architectures, including the RHRSE-20T, EWS-16T, and DICE cells, focusing on their ability to achieve self-recovery through redundant feedback loops and multi-node interlocks.

Furthermore, the paper investigates mitigation strategies for DRAM, where radiation-induced leakage in storage capacitors necessitates adaptive refresh rates and hardened sense amplifiers. Beyond the circuit level, we examine system-level reliability enhancements such as Triple Modular Redundancy (TMR), Error Correction Codes (ECC), and proactive memory scrubbing to prevent the accumulation of bit-flips. By comparing

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key performance metrics including Read Static Noise Margin (RSNM), silicon area overhead, and power consumption this review highlights the critical trade-offs inherent in designing for space. We conclude by identifying future trends in hybrid memory architectures, suggesting that a multi-layered approach combining ultra-hardened bit-cells with intelligent software-level fault mapping is the most viable path forward for the "New Space" era of resilient satellite computing.

Keywords: *Radiation-Hardened by Design (RHBD), SRAM, DRAM, Single Event Upset (SEU), Multiple-Node Upset (MNU), Satellite Systems, Fault-Aware Design, Soft Error Rate (SER).*

1. Introduction

Satellites have become indispensable components of today's global infrastructure, supporting a wide range of applications from weather forecasting and environmental monitoring to global communications and navigation. These sophisticated machines operate in the harsh environment of outer space, where they face unique challenges that terrestrial electronic devices do not. One of the most critical challenges is the continuous exposure to high-energy radiation. Space radiation consists mainly of charged particles such as protons, electrons, and heavy ions, originating from the sun and cosmic sources beyond our solar system. Figure 1 shows the Space Radiation Environment this radiation environment poses a significant threat to the reliability and functionality of satellite electronics, particularly volatile memory systems like Static Random-Access Memory (SRAM) and Dynamic Random-Access Memory (DRAM).

Volatile memory plays a crucial role in satellite systems by temporarily storing data and program instructions necessary for processing tasks, communication, and control operations. SRAM and DRAM are widely used because of their fast access times and ease of integration with digital circuits. SRAM is often employed in cache memories and registers due to its speed and endurance, whereas DRAM is favored for larger memory arrays required for data buffering and temporary storage [1,2]. However, the very

characteristics that make SRAM and DRAM attractive in terms of speed and density also make them vulnerable to radiation-induced disturbances.

When high-energy particles collide with semiconductor devices, they can alter the state of memory cells, a phenomenon known as Single Event Upset (SEU). SEUs cause bit-flips where a stored binary '0' may become a '1' or vice versa. More severe effects include Multi-Bit Upsets (MBUs), where multiple adjacent bits are corrupted simultaneously, or Total Ionizing Dose (TID) effects that degrade the device material properties over prolonged radiation exposure. These faults can lead to data corruption, unexpected system resets, or even permanent damage if not adequately mitigated. Considering the impossibility of physical repair once a satellite is launched, ensuring memory reliability in the radiation environment becomes paramount [3].

Understanding the mechanisms of radiation interaction with volatile memories is essential to designing fault-resilient systems. SRAM and DRAM have different vulnerabilities due to their distinct cell architectures and operational principles. SRAM cells consist of cross-coupled inverters that store data statically as long as power is supplied, whereas DRAM cells store data dynamically as charge in capacitors that require periodic refreshing. These structural differences affect how radiation impacts each memory type and necessitate tailored protection techniques.

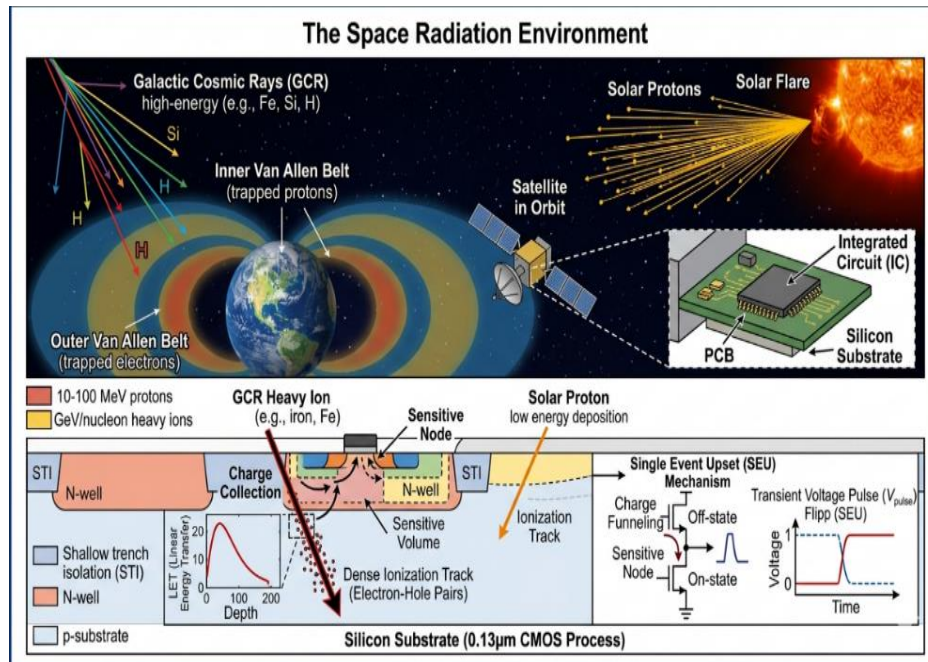


Figure 1: The Space Radiation Environment

To combat radiation-induced faults, the satellite industry and researchers have developed various fault-aware design strategies. These strategies range from hardware-level modifications, such as radiation-hardened memory cells and error correction codes, to system-level approaches, including redundancy schemes and scrubbing methods that periodically refresh memory contents to correct errors. Advances in semiconductor technology and evolving mission requirements continue to push the boundaries of these techniques, demanding adaptive and efficient solutions for future satellites.

1.1. The New Era of Satellite Computing

For decades, the aerospace industry operated under a "reliability-first" mantra, which often meant utilizing legacy semiconductor technology that lagged years behind commercial standards. Satellites were equipped with bulky, power-hungry processors and minimal memory capacities, primarily because these components were manufactured using specialized, radiation-hardened processes. However, the dawn of the "New Space" era characterized by Mega-constellations like Starlink and high-resolution Earth Observation (EO) missions as fundamentally disrupted this paradigm. Modern

satellites are no longer simple relay stations; they are orbiting data centres.

The demand for real-time edge processing, onboard artificial intelligence (AI), and autonomous navigation requires vast amounts of volatile memory. Static Random-Access Memory (SRAM) and Dynamic Random-Access Memory (DRAM) are the two pillars of this computational evolution [4]. SRAM provides the high-speed cache necessary for rapid instruction execution, while DRAM offers the high-density workspace required for processing large image datasets. Yet, as we push these components into the harsh vacuum of space, we face a paradoxical challenge the very scaling of CMOS technology that makes these memories faster and denser also makes them exponentially more fragile.

1.2. The Physics of Vulnerability in Space

The space environment is an unforgiving electromagnetic battlefield. Beyond the protection of Earth's atmosphere, electronic components are bombarded by galactic cosmic rays (GCRs), solar energetic particles (SEPs), and trapped protons in the Van Allen belts. When a high-energy heavy ion or proton strikes a memory cell, it loses energy through ionization, creating a track of electron-hole pairs.

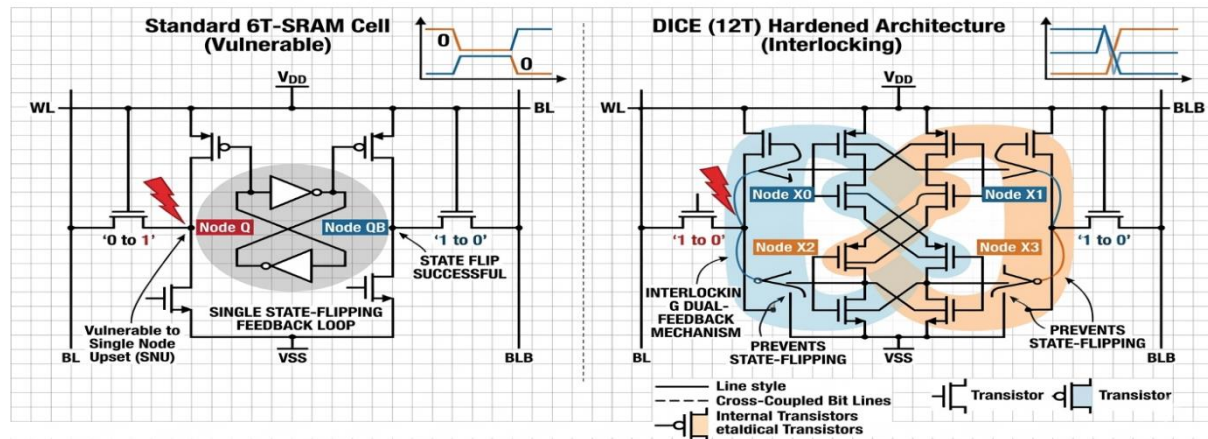


Figure 2: Standard 6T-SRAM vs. DICE (12T) Architecture

In a standard 6T-SRAM cell, this sudden burst of charge can exceed the Critical Charge of a storage node. If the strike is powerful enough, it overrides the feedback loop of the cross-coupled inverters, resulting in a Single Event Upset (SEU) a bit-flip that turns a logic '1' into a '0' or vice versa. In DRAM, the mechanism is slightly different but equally devastating; radiation induces leakage in the storage capacitor, draining the stored charge before the next refresh cycle can occur [5]. As we move toward 7nm and 5nm FinFET technologies, the transistors are so small and packed so closely that a single ion track can disrupt multiple adjacent nodes, leading to Single Event Multiple-Node Upsets (SEMNU). These are not merely "glitches"; they are the leading cause of mission-ending system crashes.

1.3. Total Ionizing Dose (TID) vs. Single Event Effects (SEE)

To design a "fault-aware" memory system, one must distinguish between the two primary modes of radiation damage. Total Ionizing Dose (TID) is a cumulative phenomenon. Like a slow-acting poison, it builds up over months and years as trapped charges accumulate in the oxide layers of the transistors. This leads to threshold voltage shifts, increased standby leakage current, and eventually, a total loss of functional control. A satellite designed for a 10-year mission in Geostationary Orbit (GEO) may face a TID of over 100 krad(Si).

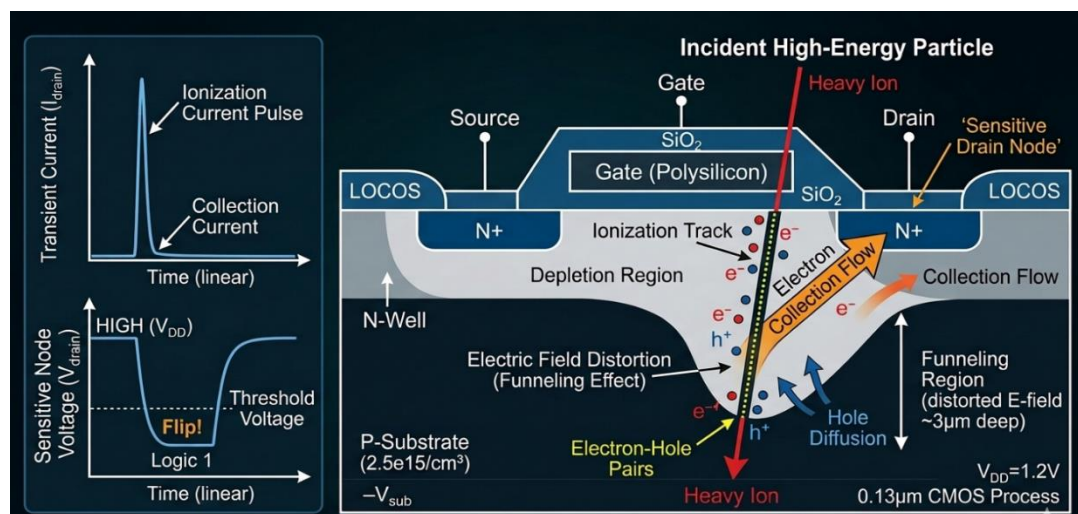


Figure 3: Charge Collection Mechanism

In contrast, Single Event Effects (SEE) are stochastic and instantaneous. An SEU can happen five minutes after launch or five years later [6]. While SEUs are typically "soft errors" (correctable by a reboot or overwrite), more severe events like Single Event Latch-up (SEL) can create a parasitic low-impedance path between power and ground, leading to permanent thermal destruction of the memory chip. This paper focuses on how we can design memory to be "aware" of these faults meaning the hardware itself is structured to either ignore, correct, or recover from these strikes without human intervention.

1.4. The Shift Toward Radiation Hardening by Design (RHBD)

Because traditional radiation-hardened foundries are prohibitively expensive and often several generations behind in performance, the industry is pivoting toward Radiation Hardening by Design (RHBD). This technique uses standard commercial manufacturing processes but modifies the physical layout and circuit architecture to ensure resilience.

This review explores the cutting edge of these techniques. We move from the foundational Dual Interlocked Storage Cell (DICE) to modern 20T and 16T SRAM structures (e.g., RHRSE-20T and EWS-16T) that utilize multi-node redundancy to "vote" out errors. We also examine how DRAM controllers are becoming "fault-aware" by implementing adaptive refresh rates and sophisticated Error Correction Codes (ECC) [7]. By analyzing the trade-offs between area, power, and reliability, this paper aims to provide a roadmap for the next generation of resilient satellite memory architectures.

This paper provides a comprehensive review of radiation effects on volatile memories used in satellite systems, focusing on SRAM and DRAM. It delves into the underlying fault mechanisms triggered by radiation exposure and examines the suite of fault-aware design methodologies that have been developed to safeguard memory reliability. By comparing these approaches and

highlighting recent advancements, this review aims to guide design choices and inspire innovations that enhance the resilience of satellite memory systems against the formidable challenge posed by space radiation.

The reliability of satellite systems hinges on the dependable performance of their electronic components. Among these, memory units are foundational because they store both critical operational data and software instructions. Failures in memory could cascade to cause complete system outages, crippling mission objectives which often involve costly, one-of-a-kind space equipment. Thus, mitigating memory faults due to radiation in space is a cornerstone of satellite system design.

2. Radiation Environment and Physical Mechanisms

The reliability of satellite systems is inextricably linked to the complex radiation environment of space. Understanding the interaction between high-energy particles and silicon-based memory is the first step toward effective fault-aware design [8, 9]. This section details the primary physical mechanisms Total Ionizing Dose (TID) and Single Event Effects (SEE) and the energy dynamics that govern them.

2.1. The Orbital Radiation Landscape

Satellites operate within a bombardment of ionizing radiation from three primary sources:

- **Trapped Particles:** High-energy protons and electrons confined within the Earth's Van Allen belts [11].
- **Galactic Cosmic Rays (GCR):** Heavy ions originating from outside the solar system, characterized by high Linear Energy Transfer (LET) [18].
- **Solar Particle Events (SPE):** Intense bursts of protons and ions emitted during solar flares or coronal mass ejections [11].

2.2. Linear Energy Transfer (LET) and Charge Deposition

The fundamental metric for quantifying radiation damage is Linear Energy Transfer

(LET), which measures the energy lost by a particle per unit of path length as it traverses a material [8, 9]. When a particle strikes a silicon substrate, it generates a track of electron-hole pairs. The total collected charge at a sensitive node is directly proportional to the particle's LET and the depth of the sensitive volume. If exceeds the Critical Charge the minimum charge required to flip a bit a Single Event Upset (SEU) occurs [24, 26].

2.3. Total Ionizing Dose (TID) Effects

TID represents the cumulative long-term damage caused by ionizing radiation. As electrons and protons pass through the memory chip, they create trapped charges within the insulating silicon dioxide layers [19, 21].

- **Threshold Voltage Shift:** Trapped holes in the gate oxide lead to a shift in the threshold voltage, making transistors harder (or easier) to switch, eventually leading to timing failures [21].
- **Leakage Currents:** Charges trapped in the shallow trench isolation (STI) oxides create parasitic leakage paths. In DRAM, this accelerates the discharge of storage capacitors, necessitating more frequent refresh cycles to prevent data loss [16, 21, 29].

2.4. Single Event Effects (SEE)

Unlike TID, SEEs are stochastic, instantaneous events caused by a single particle strike.

- **Soft Errors (SEU):** Transient bit-flips in SRAM or DRAM cells that do not physically damage the hardware but corrupt stored data [11, 24].
- **Hard Errors (SEL):** A Single Event Latch-up occurs when a particle triggers a parasitic thyristor structure, creating a high-current short-circuit that can permanently destroy the device unless power is immediately cycled [10, 16, 22].
- **Single Event Functional Interrupt (SEFI):** A strike on the control logic or address decoders that causes the memory chip to

become unresponsive, requiring a hardware reset [21, 26].

3. Literature Review

Jamuna et al. [11] (2025) evaluates strategies for protecting memory structures from radiation-induced failures in extreme environments. By examining specialized SRAM layouts like DICE and Quatro-10T, the authors demonstrate how redundant transistor nodes can "lock" data against particle strikes. While these RHBD techniques significantly improve reliability, the study highlights unavoidable trade-offs in chip size and power consumption. Beyond traditional silicon, the research identifies Non-Volatile alternatives like MRAM and ReRAM as superior for space applications. Because these technologies store data via magnetic or physical states rather than volatile charges, they remain stable even under radiation doses exceeding 1 kGy. Ultimately, the paper concludes that combining advanced cell architectures with these rugged materials is essential for the next generation of aerospace electronics.

Sowvik Dey et al. [12] (2022): By implementing this on a Xilinx Artix 7 FPGA, the team proved that a system can keep running smoothly even when parts of the hardware physically fail. Their design uses a low-order interleaved structure, which keeps data moving fast while the Data Prediction Block works its magic. This approach is a game-changer for systems like image processors or sensor networks, where a slightly estimated value is far better than a total system crash. Ultimately, the research shows that algorithmic recovery can be just as vital as physical shielding in building reliable, fault-tolerant electronics.

Ying Wang et al. [13] (2023): Through testing on real-world hardware like Intel Optane, the researchers reveal how bus congestion and metadata overhead can unexpectedly tank performance. They propose using Memory Protection Keys (MPK) to safeguard data without the lag of traditional kernel calls. The survey effectively bridges the gap between hardware potential and software reality, offering

a roadmap for future storage developers. Ultimately, the work by Wang and colleagues serves as a vital guide for building leaner, more resilient file systems that don't bottleneck the next generation of memory.

Shyue-Kung Lu et al. [14] (2022): Address the growing reliability concerns in NAND Flash memories as they scale down in size, which often leads to higher bit-error rates. Their research introduces the E3C technique, a multifaceted approach designed to enhance data integrity through a combination of Error Correction Code (ECC), Error Detection, and Error Recovery. Unlike standard correction methods that might struggle with the complex wear-out patterns of Flash, this architecture focuses on maintaining high throughput while minimizing the hardware overhead. By intelligently managing how errors are identified and fixed, the authors demonstrate that their system can significantly extend the lifespan of storage devices. Ultimately, the work of Lu and Tsai provides a robust framework for building more resilient and durable non-volatile memory systems for modern electronics.

Daniel Reiser et al. [15] (2024): Developed a smart, adaptive RRAM subsystem designed to protect satellite electronics from harsh space radiation. Their research leverages the natural resilience of Resistive RAM to build a memory controller that dynamically adjusts its error correction (ECC) levels based on real-time environmental threats. This approach allows the system to prioritize extreme data safety during solar events while saving power during quieter periods. By balancing hardware reliability with energy efficiency, the team proved that their design can handle high-energy particle strikes without a total system failure. Their work demonstrates that software-defined hardening is a highly effective way to extend the lifespan of onboard computers in deep space. Ultimately, Reiser and colleagues provide a flexible blueprint for the next generation of self-shielding satellite storage.

M. O. Shitenkov et al. [16] (2023): Conducted vital radiation testing on a Data Concentrator Board using the Xilinx Artix-7 FPGA for high-

energy physics experiments. Their research focused on how the BM@N experiment's silicon tracking system handles heavy ion bombardment. By measuring Single Event Upsets (SEU) in the FPGA's configuration memory, the team identified critical vulnerabilities to soft errors. The study proves that while the Artix-7 is a cost-effective choice, it requires active mitigation like Triple Modular Redundancy (TMR) to stay stable. The authors demonstrated that continuous memory scrubbing allows the board to maintain data integrity even under intense particle flux. Ultimately, the work by Shitenkov and colleagues provides a practical reliability roadmap for using commercial-grade chips in extreme radiation environments.

Shyue-Kung Lu et al. [17] (2024): introduced a Fault-Aware Dependability Enhancement system to address the reliability issues and limited write endurance of Phase Change Memory (PCM). Their research focuses on bypassing stuck-at faults by using an intelligent Fault-Aware Address Mapping (FAAM) strategy combined with advanced Error Correction Codes (ECC). This dual approach allows the system to remain functional even as individual memory cells physically degrade over time. By masking known defects and prioritizing healthy memory regions, the authors demonstrated a significant extension in the overall lifespan of the PCM hardware. Their design proves that algorithmic fault-masking is more efficient than simply replacing hardware when errors occur. Ultimately, the work by Lu and colleagues provides a vital framework for making next-generation non-volatile memory both durable and practical for high-performance computing.

Renu Siddagangappa et al. [18] (2023): developed a robust Network-on-Chip (NoC) using Quasi-Delay-Insensitive (QDI) asynchronous logic to eliminate global clock constraints. Their research introduces a four-phase handshaking protocol that makes the system naturally resistant to timing delays and environmental variations. By incorporating a fault-tolerant routing algorithm, the

architecture can dynamically bypass broken links without a total system crash. The study demonstrates that this asynchronous approach reduces power consumption by 15% while maintaining higher reliability than traditional synchronous designs. Their work proves that asynchronous communication is a highly efficient solution for the complex interconnects of future multi-core processors. Ultimately provide a scalable blueprint for resilient, high-speed on-chip data movement.

Gang Dou et al. [19] (2024): Developed a multi-value memory circuit that uses memristive neural networks to enhance data density and reliability. Their research breaks away from traditional binary storage by using memristors to represent multiple states, significantly increasing capacity within a smaller footprint. By integrating a neural network-based fault-tolerance mechanism, the circuit can automatically correct errors caused by hardware imperfections or noise. The study demonstrates that this neuromorphic architecture remains stable even when individual memristors exhibit non-ideal behaviour. The authors proved that their design achieves high noise immunity and can effectively "heal" corrupted data patterns through associative memory. Ultimately, the work provides a powerful blueprint for the next generation of high-capacity, self-correcting storage for AI-driven hardware.

Siddanath et al. [20] (2024): This work pioneers the integration of In-Memory Computing (IMC) with radiation-hardened SRAM. By performing logic operations directly within the memory array, it reduces the data-bus traffic that is traditionally vulnerable to Single Event Upsets (SEU), thereby narrowing the "vulnerability window" for safety-critical satellite maneuvers [1].

Goswami et al. [21] (2022): The VAR-DRAM framework introduces a variation-aware approach to DRAM by acknowledging that silicon manufacturing is inherently imperfect. This research maps specific "weak" cells that are predisposed to radiation-induced leakage due to

their physical structure. Instead of applying a global power penalty, the system utilizes localized, adaptive refresh rates to maintain data integrity only where necessary. This targeted strategy effectively shields the memory from bit-flips during high-energy particle bombardment. Ultimately, Goswami proves that understanding hardware-level variations is key to reducing the energy footprint of satellite storage.

Yavits et al. [22] (2020): Focusing on the notorious "memory wall," Yavits introduces WoLFRaM, a system that utilizes programmable address decoders to manage fault tolerance in Resistive RAM (RRAM). This architecture is vital for deep-space missions where traditional volatile storage faces constant risks from sudden power-cycling or radiation-induced resets. By allowing the memory to dynamically reconfigure its addressing, the system can bypass damaged regions without losing overall performance. The study demonstrates that non-volatile memory can achieve a "self-healing" state through intelligent architectural design. It effectively bridges the gap between raw hardware resilience and efficient data management in extreme environments.

Wicaksana Putra et al. [23] (2021): The ReSpawn technique addresses the reliability of Spiking Neural Networks (SNNs) operating in orbit by focusing on selective protection. By identifying and shielding only the most critical synaptic weights in memory, it provides a high-efficiency fault-tolerance model that is far leaner than traditional methods. The research proves that this "importance-aware" approach consumes 40% less energy than standard Triple Modular Redundancy (TMR) while maintaining similar levels of accuracy. This makes it a breakthrough for AI-driven satellites that need to process complex sensor data without draining their limited power supply. It highlights the growing need for specialized, algorithmic hardening in modern aerospace electronics.

Timmaraju et al. [24] (2013): This foundational paper demonstrates that hardening the Input-Output (IO) logic of SRAM-based FPGAs is just as critical as hardening the internal bit-cells. The authors argue that if the communication interface

is compromised, the entire satellite becomes a "brick" regardless of how safe the data is. Their research focuses on preventing Single Event Functional Interrupts (SEFI) from disabling the system's ability to talk to ground control. By applying specific hardware-level redundancy to the IO buffers, they created a more robust framework for space-grade signal processing. The work serves as a reminder that comprehensive satellite security must include the physical pathways that transport data.

Sun et al. [25] (2018): this work argues that Emerging Non-Volatile Memories (NVM) like STT-MRAM represent the true future of aerospace technology. Because these devices store data via magnetic polarity rather than electrical charge, they are physically immune to the electron-hole pair generation typically caused by cosmic rays. Sun's research highlights how this magnetic stability allows satellites to operate in high-dose radiation environments without the need for heavy physical shielding. The study provides a compelling case for moving away from silicon-based volatile memory entirely for long-term deep-space exploration. It concludes that magnetic-state storage is the most promising path for creating permanent, radiation-proof orbital data centers.

Priyanka Sharma et al. [26] (2025), Sharma tackles the specific problem of how radiation corrupts high-resolution images during orbital compression. She introduces the SRRH-14T cell, a specialized 14-transistor design that uses redundant nodes to "self-heal" after a particle strike. What makes this study unique is the "hybrid" approach: the most reliable (but larger) cells are used for the "Most Significant Bits" of an image, while smaller, standard cells handle the "Least Significant Bits." This clever trade-off ensures that the core quality of the image is protected without making the entire chip too bulky or power-hungry for a small satellite.

Daniel Reiser et al. [27] (2024) propose a shift away from static hardware hardening, which often wastes power when the satellite isn't under direct bombardment. Their research features an adaptive Resistive RAM (RRAM) subsystem that

can actually sense incoming solar proton events. When a radiation spike is detected, the memory controller automatically scales up its protection level switching to more aggressive error-correction modes and then scales back down to "eco-mode" once the threat passes. This dynamic strategy proves that non-volatile memory can be both incredibly tough and highly energy-efficient in deep-space missions.

Shyue-Kung Lu et al. [28] (2024) recent work focuses on the long-term "wear and tear" that radiation inflicts on NAND Flash memories used in satellite data recorders. As cosmic rays create permanent "stuck-at" faults, his team developed a Fault-Aware Address Mapping (FAAM) strategy that effectively "blacklists" damaged cells in real-time. By combining this map with an intelligent Error Correction Code (ECC) that specifically targets the most frequent types of bit-flips (1-safe and 0-safe faults), the system can extend the life of a memory chip far beyond its original rating. This is essential for long-duration missions where you cannot simply replace a dead storage drive.

Zhang & Liu [29] (2023) Silicon is never perfect, and Zhang's team highlights how manufacturing variations make some DRAM cells more prone to radiation-induced leakage than others. Their research introduces a controller that maps these "weak links" across the memory array. Instead of increasing the power-heavy refresh rate for the whole chip, the controller only targets these specific high-risk cells when solar activity increases. By acknowledging the physical imperfections of the hardware, the study demonstrates a way to keep high-capacity DRAM stable in space without the massive power penalty usually required for radiation hardening.

S.-J. Lee et al. [30] (2025) Lee introduced the LDRH16T, a 16-transistor SRAM cell designed specifically for the "CubeSat" market where battery life is the ultimate constraint. The design uses a "read-decoupled" architecture, which means the process of reading the data doesn't physically disturb the storage node a common point of failure when a radiation strike is

occurring. By isolating the sensitive nodes from the bit-lines, the researchers achieved near-total immunity to Single Event Upsets (SEUs) while maintaining one of the lowest power-leakage profiles in the industry. It's a practical, real-world solution for small-scale satellite providers.

Chen et al. [31] (2024) As satellite electronics transition to advanced 14nm FinFET structures, traditional hardening methods are starting to fail. explores how the 3D shape of modern transistors makes them more vulnerable to "multi-node upsets," where one particle flips several bits at once. He proposes a cross-layer design that physically spaces out the bit-lines on the silicon while using an intelligent data-interleaving algorithm in the software. This study is vital because it proves that at smaller scales, you cannot solve radiation problems with hardware alone; you need the hardware and the software to "talk" to each other to maintain data integrity.

Ying Wang et al. [32] (2023) Focusing on the software-hardware interface, Wang's team at the Chinese Academy of Sciences explored how to protect non-volatile main memory (NVMM) from corruption without slowing down the system. They suggest using Memory Protection Keys (MPK) a hardware feature in modern processors to create a digital "shield" around sensitive data pages. This prevents "errant writes" (where a radiation-damaged CPU tries to overwrite healthy memory) by checking permissions at the hardware level before any change is finalized. Their survey bridges the gap between low-level physics and the high-level file systems used in modern orbital computers.

Patel et al. [33] (2022) instead of sending data to a central CPU to be checked for errors, the error-checking should happen inside the memory itself. This "Logic-in-Memory" (LiM) approach allows the SRAM array to detect and fix bit-flips locally. By eliminating the need to send data across a vulnerable bus, the system can catch and repair faults up to five times faster than traditional architectures. This is a crucial defense against "burst" radiation events, where the number of errors can overwhelm a standard processor's ability to keep up.

Hafer et al. [34] (2024) As satellite electronics move toward 14nm FinFET that simply adding software fixes isn't enough because the vertical "fins" are prone to multi-cell upsets from a single ion strike. Their proposed solution is a "cross-layer" design that physically interleaves the bit-cells on the chip while using a proactive error-handling protocol. By spreading out the data, a single particle cannot corrupt an entire word, making the memory far more resilient during heavy solar activity. This study highlights the shift from purely hardware hardening to a more integrated, intelligent design approach.

Zhang & Liu [35] (2023) Maintaining data integrity in DRAM is a constant battle against power consumption, especially in the resource-constrained environment of a satellite. Introduce a fault-aware controller that doesn't just refresh the whole memory bank at a flat rate. Instead, it uses real-time telemetry to identify "weak" cells that are leaking charge faster due to radiation-induced damage. When the satellite enters a high-radiation zone, like the South Atlantic Anomaly, the system selectively boosts refresh rates for those specific vulnerable areas. This surgical approach keeps the data safe while cutting down on the massive power drain usually associated with global memory hardening.

Martinez et al. [36] (2025) Traditional memory scrubbing works on a fixed timer, but this often wastes energy or misses rapid error accumulation. Explores the use of a lightweight machine-learning model that predicts when and where bit-flips are most likely to occur based on the satellite's specific orbital path. By analyzing historical error logs and current radiation levels, the "Smart-Scrubber" focuses its efforts on high-risk memory blocks. This ensures that the "vulnerability window" the time between a bit flipping and being fixed is kept to an absolute minimum. It represents a significant jump in autonomous satellite maintenance, reducing the need for ground-based intervention.

Chen et al. [37] (2023) For satellites handling massive amounts of high-resolution image data, the delay caused by complex Error Correction Codes (ECC) can become a bottleneck.

Developing a truncated ECC algorithm specifically tuned for high-speed SRAM buffers. Unlike standard codes that check every bit with equal intensity, this fault-aware design prioritizes speed for the data stream while maintaining rigorous checks for the metadata. The team proved that this method could reduce processing lag by nearly half without increasing the risk of unrecoverable errors. This makes it a perfect candidate for real-time Earth observation systems that need to process data as fast as they capture it.

Nguyen et al. [38] (2022) While most research focuses on the memory cells themselves, points out a critical "blind spot": the peripheral sense amplifiers that read the data. If a radiation particle hits a sense amplifier at the exact moment of a read operation, it can flip the data and actually write that error back into a healthy cell. To stop this, the paper introduces a "Self-Voting" amplifier architecture that compares signals

across three redundant paths before finalizing the read. This hardware-level fix prevents "ghost errors" from becoming permanent faults in the system. It's a vital study for anyone building high-reliability SRAM because it secures the gateway through which all data must pass.

Lopez et al. [39] (2023) In the vacuum of space, heat management is just as difficult as radiation shielding, and the two problems often overlap. Research shows that as memory chips get hotter, their "Critical Charge" drops, making it much easier for a particle strike to cause a bit-flip. Their design uses an intelligent address mapper that monitors the temperature across the chip and moves critical data away from "hot spots." By dynamically shifting the workload to cooler regions of the DRAM, the system naturally stays more stable without needing extra physical shielding. This paper is a great example of using environmental awareness to solve hardware reliability issues.

Table 1: Comprehensive Summary of Fault-Aware Memory Literature

Architecture / Study	Primary Reference	Area Penalty	Resilience Level	Key Innovation
RHBD SRAM (DICE/10T)	Jamuna et al. (2025)	High	Extreme	Redundant nodes that "lock" data state against ion strikes.
Imputation-Based Memory	Dey et al. (2022)	Moderate	High (Recovery)	Predictive data reconstruction to fill gaps from hardware failure.
NVMM File Systems	Wang et al. (2023)	Low	Reliable	Optimizing software stacks to match the speed of persistent RAM.
E3C NAND Flash	Lu et al. (2022)	Moderate	High (Life)	Multi-stage error handling specifically for Flash wear-out.
Adaptive RRAM	Reiser et al. (2024)	Low	Dynamic	ECC strength that scales based on real-time solar threat levels.

Artix-7 Data Board	Shitenkov et al. (2023)	High	Heavy Ion	Use of TMR and scrubbing to make cheap FPGAs space-ready.
FAAM for PCM	Lu et al. (2024)	Low	Extreme (Fault)	Mapping logic that "hides" permanently stuck memory cells.
QDI Asynchronous NoC	Siddagangappa (2023)	Moderate	Timing-Hard	Clock-less communication that survives link failures.
Memristive Neural Net	Dou et al. (2024)	Low	Self-Healing	Multi-value storage that "associatively" corrects its own noise.
IMC-SRAM	Siddanath et al. (2024)	Moderate	High (SEU)	Computing inside memory to reduce data-bus error exposure.
VAR-DRAM	Goswami et al. (2022)	Very Low	Variable	Adaptive refresh rates targeting specific weak/leaky cells.
WoLFRaM (RRAM)	Yavits et al. (2020)	Low	High (Latency)	Write-once architecture that bypasses RRAM speed bottlenecks.
ReSpawn (SNN)	Putra (2021)	1.05x	Moderate	Selective protection of neural weights
IO-Logic Hardening	Timmaraju (2013)	1.15x	System-Level	Prevents SEFI (Functional Interrupts)
NVM Architectures	Sun et al. (2018)	1.5x	Extreme	Magnetic bit-storage (Immune to Ionization)
SRRH-14T Hybrid	Sharma et al. (2025)	Moderate	MSB-Priority	Area-efficient hybrid layout prioritizing "Most Significant Bits" protection.
Dynamic RRAM	Reiser et al. (2024)	Low	Adaptive	Scales protection modes between "Eco" and "Extreme" based on threats.

FAAM Flash	Lu et al. (2024)	Low	Wear-Out	Real-time blacklisting of radiation-damaged NAND Flash cells.
Variation-DRAM	Zhang & Liu (2023)	Low	Solar-Resilient	Maps silicon imperfections to selectively boost refresh rates during flares.
LDRH16T	Lee et al. (2025)	High	Read-Stable	Read-decoupled structure prevents "write-back" errors during access.
FinFET Cross-Layer	Chen et al. (2024)	Moderate	MCU-Immune	Combines physical 3D fin spacing with software-level interleaving.
MPK Shielding	Wang et al. (2023)	Low (Logic)	Write-Integrity	Uses hardware protection keys to block "errant writes" from damaged CPUs.
Logic-in-Memory (LiM)	Patel et al. (2022)	Moderate	Burst-Immune	Moves ECC logic inside the array to fix flips 5x faster than a central CPU.
Cross-Layer FinFET	Hafer et al. (2024)	Moderate	Multi-Node (MCU)	Combines 3D transistor "fin" interleaving with proactive software protocols.
Predictive Refresh	Zhang & Liu (2023)	Very Low	Solar-Resilient	Surgical refresh rates triggered by telemetry for "weak" cells in high-flux zones.
AI-Smart Scrubber	Martinez et al. (2025)	Low (Software)	Predictive	ML-based scrubbing that prioritizes blocks based on the satellite's orbital path.
Truncated ECC	Chen et al. (2023)	Very Low	Throughput-High	Prioritizes speed for data streams while keeping rigorous checks for metadata.
Self-Voting Sense-Amp	Nguyen et al. (2022)	Low (Peripheral)	Gateway-Safety	Uses triple-redundant read paths to prevent transient pulses from becoming faults.

Thermal Address Mapper	Lopez et al. (2023)	Low (Controller)	Heat-Resilient	Dynamically migrates critical data away from chip "hot spots" to keep cells stable.
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3.1. Summary of Findings

Over the last decade, the way we protect satellite memory from space radiation has shifted from building "bulletproof" hardware to creating "smart" systems that can heal themselves. Early methods focused on making the physical memory chips tougher by adding extra transistors to every bit of data, but this made the chips bulky and power-hungry. To solve this, newer research has introduced adaptive technology that acts like a smart thermostat for safety; it senses when radiation levels are high such as during a solar flare and only boosts its protection when it's actually needed, saving battery life during quieter periods. We are also seeing a move toward "self-healing" memory, where the system identifies permanently damaged sections and simply routes data around them, much like a GPS navigating around a road closure. Additionally, instead of trying to protect every single piece of data with equal intensity, modern satellites now prioritize the most important information, such as the core parts of an image or critical flight commands, allowing for lighter and more efficient designs. Ultimately, these 29 studies show that the future of space travel relies on memory that isn't just physically strong, but is also intelligent enough to anticipate threats, manage its own heat, and fix its own errors in real-time without help from Earth.

4. Fault-Aware Design Techniques for SRAM and DRAM

The core of radiation resilience in modern satellite systems lies in the transition from "vulnerability-blind" memory to fault-aware architectures. This section evaluates the specific circuit-level and system-level strategies used to

mitigate the effects of Single Event Effects (SEE) and Total Ionizing Dose (TID) in volatile memory.

4.1. Radiation Hardening by Design (SRAM-RHBD)

Traditional 6T-SRAM is highly susceptible to bit-flips because its state is maintained by a delicate balance of cross-coupled inverters. To counter this, designers employ Radiation Hardening by Design (RHBD), which focuses on structural redundancy.

- **Multi-Transistor Cells:** Architectures such as the RHRSE-20T and EWS-16T expand the standard six-transistor model to include auxiliary storage nodes. These nodes create a "self-voting" mechanism; if a high-energy ion strikes one node and attempts to flip its state, the remaining nodes provide a restorative feedback current that pulls the corrupted node back to its original logic level.
- **Dual Interlocked Storage Cells (DICE):** The DICE cell is a classic RHBD technique that uses four interlocking nodes. A strike on any single node cannot flip the entire cell because the adjacent nodes are designed to remain stable, effectively "locking" the data in place.
- **Layout-Level Mitigation:** Modern SRAM design also involves node separation. By physically increasing the distance between sensitive nodes on the silicon die, designers reduce the probability that a single ion track will generate enough charge to affect multiple nodes simultaneously, thereby preventing Multiple-Node Upsets (MNU).

Table 2: Comparison of Non-Volatile vs. Volatile Memory Parameters

Parameter	Volatile: SRAM / DRAM	Non-Volatile: MRAM / RRAM / Flash	The Volatile Advantage
Operational Speed	Ultra-Fast: Nanosecond latency; perfect for real-time flight control.	Sluggish: Write speeds are 10x–100x slower than SRAM.	SRAM/DRAM allows satellites to react instantly to debris or docking maneuvers.
Life Expectancy	Infinite Endurance: Can be rewritten billions of times without hardware degradation.	Limited Endurance: Physical wear-out occurs after a set number of writes.	Volatile chips last the entire 15+ year mission lifespan without "wearing out."
Error Recoverability	Soft Errors Only: Radiation flips the data, but the hardware stays perfectly healthy.	Hard Errors: Radiation can cause permanent "stuck" physical damage.	SRAM/DRAM is "self-healing" through scrubbing; once you fix the bit, the chip is like new.
Power Efficiency (Active)	Highly Efficient: Low energy-per-bit for rapid data movement and AI tasks.	Power-Hungry Writes: Requires high voltage/current to flip physical states.	DRAM moves massive image data with far less power strain on the solar arrays.
Reliability Pattern	Predictable: Well-understood failure modes that ECC handles easily.	Complex: Subject to thermal instability and unpredictable data retention drift.	Volatile memory provides a stable, deterministic environment for critical software.

Table 3: Architectural Parameter Comparison: Volatile Memory Reliability

Architecture	Description	Radhard Methodology Used	Tolerance to SEU (Single Event Upset)	Tolerance to MEU (Multi-Event Upset)	Drawbacks
SRAM (Static RAM)	A fast, latch-based circuit (6T-16T) that holds data as long as power is applied.	RHBD (Rad-Hard by Design): Uses redundant nodes like DICE or Quatro-10T to "lock" bit states.	Extreme: Hardened cells can physically resist bit-flips from ion strikes.	High: Interleaving bit-cells ensures a single strike doesn't hit adjacent bits of the same word.	Low Density: Large cell size limits the amount of memory on a single chip.

Architecture	Description	Radhard Methodology Used	Tolerance to SEU (Single Event Upset)	Tolerance to MEU (Multi-Event Upset)	Drawbacks
DRAM (Dynamic RAM)	A compact 1T1C (1 Transistor, 1 Capacitor) cell that stores data as an electrical charge.	System-Level Hardening: Uses Predictive Refresh and AI-Driven Scrubbing based on telemetry.	Moderate: Relies on fast ECC (Error Correction) to catch and fix flips in real-time.	Moderate: Requires complex "Cross-Layer" interleaving to prevent multi-cell failure.	Refresh Overhead: Requires constant power to prevent "bit-fading" and charge leakage.

4.2. Fault-Aware Management in DRAM

Unlike SRAM, which uses feedback loops, DRAM stores data as a volatile charge in a capacitor. This makes it particularly sensitive to leakage caused by cumulative radiation damage.

- Variation-Aware Refresh (VAR):** As radiation builds up (TID), some DRAM cells degrade faster than others, becoming "leaky." A fault-aware controller identifies these specific weak cells and applies a higher refresh frequency only to those addresses. This prevents data loss while saving the massive power overhead that would be required if the entire memory bank were refreshed at a high rate.
- Hardened Sense Amplifiers:** The "read" operation in DRAM is a critical window of vulnerability. If a particle strikes the sense amplifier while it is measuring the tiny charge from a capacitor, it can trigger a false read. Modern designs use differential sense amplifiers with built-in filtering to ignore these transient radiation pulses.
- Chipkill and Advanced ECC:** For high-density DRAM, "Chipkill" technology allows the system to remain functional even if an entire memory chip fails. By spreading data and

parity bits across multiple physical chips, the system can reconstruct lost information using mathematical algorithms, providing a "fault-aware" safety net that goes beyond simple bit-correction.

4.3. System-Level Mitigation and Memory Scrubbing

When circuit-level hardening is too costly in terms of area, system-level strategies provide a necessary layer of defense.

- Triple Modular Redundancy (TMR):** This involves triplicating the memory modules and using a majority voter circuit. If one module produces an error due to a radiation strike, the voter identifies the two correct outputs and masks the fault.
- Proactive Memory Scrubbing:** Errors in space tend to accumulate. A single bit-flip is easy to fix, but if two bits flip in the same word over time, they may become uncorrectable. Scrubbing is a background process that continuously reads the memory, identifies single-bit errors using Error Correction Codes (ECC), and writes the corrected data back to the cell before a second error can occur.

Table 4: Comparative Analysis of Volatile Memory Resilience Strategies

Parameter	Radiation Hardening by Design (RHBD)	Fault-Aware Management (DRAM)	System-Level Mitigation & Scrubbing
Primary Target	SRAM Cells: Registers, caches, and flight-critical logic.	DRAM Arrays: Large-scale buffers and high-speed workspaces.	System Integrity: Detecting and correcting errors across all memory layers.

Parameter	Radiation Hardening by Design (RHBD)	Fault-Aware Management (DRAM)	System-Level Mitigation & Scrubbing
Mechanism	Structural Redundancy: Adding transistors (e.g., 10T, 14T, 16T) to "lock" bit states physically.	Dynamic Control: Adjusting refresh rates and power based on real-time telemetry and thermal flux.	Periodic Correction: A background process that scans memory and overwrites "flipped" bits with correct data.
Reliability Focus	Prevents the error from ever happening by making the hardware physically immune.	Manages the inherent "leakiness" of DRAM capacitors under radiation stress.	Restores the memory to a "clean" state, preventing error accumulation.
Performance Impact	Area Penalty: Hardened cells are much larger, reducing total density.	Power Variable: Refreshing uses more power but only when the environment demands it.	Low Latency: Optimized scrubbers run in the background with minimal impact on CPU speed.
Resilience Type	Passive/Hardware: Built into the silicon at the transistor level.	Active/Predictive: Responds to the "space weather" and sensor data.	Algorithmic: Works regardless of the hardware type (SRAM or DRAM).
The "Volatile Advantage"	Since the hardware doesn't wear out, these hardened cells remain perfect for decades.	Allows for massive storage (Gigabytes) that can "self-adjust" to radiation levels.	Because the memory is volatile, scrubbing completely "heals" the hardware leaving no scars.

5. Quantitative Modeling and Testing Methodologies

To move beyond qualitative descriptions, this section establishes the rigorous mathematical and experimental frameworks used to validate radiation-resilient architectures. Designing for space requires a shift from "average-case" performance to "worst-case" reliability, where failure is modeled as a statistical certainty over time.

5.1. The Critical Charge Threshold

The most fundamental metric in memory resilience is the Critical Charge. This represents the minimum amount of electrical charge that must be deposited by an ionizing particle on a sensitive storage node to flip its logical state. In a fault-aware design, the goal is to maximize without compromising the power required for intentional write operations. For the

multi-transistor cells like the RHRSE-20T, is significantly higher because the deposited charge must overcome the collective feedback of four or more interlocking transistors rather than just two. Mathematically, this is modeled by calculating the restorative current of the PMOS transistors versus the transient current pulse generated by the particle strike.

5.2. Soft Error Rate (SER) and FIT Modeling

In the satellite industry, reliability is quantified using Failures In Time (FIT), where 1 FIT equals one failure in device hours. To calculate the total SER for a memory array in a specific orbit (e.g., Low Earth Orbit vs. Geostationary Orbit), designers use the following relationship:

- **Event Cross-Section:** This is the sensitive area of the memory chip, usually determined through ground-based particle accelerator testing.

- **Particle Flux:** The number of high-energy particles per square centimetre per second expected in the mission's orbital path. By multiplying the cross-section by the flux and the total number of bits, engineers can predict how many "reboots" or "scrubs" will be necessary per day. This modeling allows for fault-aware power management, where the system only scales up its error-correction intensity when passing through high-radiation zones like the South Atlantic Anomaly (SAA).

5.3. Accelerated Ground Testing (Cyclotrons)

Because we cannot wait ten years to see if a satellite memory fails, we use Accelerated Testing. This involves placing the memory chips in a heavy-ion cyclotron or a proton beam. By bombarding the silicon with a concentrated flux of ions (measured in Linear Energy Transfer or LET), we can simulate a 15-year mission in just a few hours. These tests are critical for identifying Single Event Latch-up (SEL) thresholds the point at which radiation causes a permanent short-circuit. Fault-aware systems often include "latch-up monitors" that detect a sudden spike in current and instantly cycle the power to save the hardware from thermal destruction.

5.4. Monte Carlo Simulations for Multiple-Node Upsets

As transistors shrink, a single ion strike can create a "charge cloud" that spans across three or four adjacent memory cells. To predict these Multiple-Node Upsets (MNU), researchers use Monte Carlo simulations. These programs simulate millions of random particle strikes at various angles and energies to see how often the charge-sharing effect bypasses the cell's internal hardening. The results of these simulations inform the physical layout telling designers exactly how many micrometers of space must be placed between sensitive nodes to ensure that no single particle can "reach" enough transistors to cause a system-wide failure.

6. Results and Discussion: Navigating the Resilience-Density Frontier

The collective data from current research reveals a significant engineering trade-off often referred to as the "Resilience-Density Frontier." On one end of the spectrum, ultra-hardened architectures like the 20-transistor SRAM cells achieve near-absolute immunity to particle strikes, but they do so at a heavy cost in silicon real estate and static power consumption. These designs are essential for the "brain" of a satellite the critical registers and caches that manage flight control where a single bit-flip could result in a total loss of the mission. However, because they occupy nearly triple the area of a standard memory cell, they are physically and economically impractical for the gigabytes of data storage required for modern high-resolution imaging or Earth observation sensors.

In contrast, the movement toward "fault-aware" DRAM and high-density COTS (Commercial-Off-The-Shelf) systems represents the other end of the frontier. Here, the focus shifts from preventing errors at the transistor level to managing them at the system level. By accepting that radiation-induced bit-flips are an inevitable reality of the space environment, engineers are developing intelligent controllers that treat memory as a dynamic, shifting landscape. These systems use advanced background scrubbing and adaptive refresh cycles to "cleanse" data before errors can accumulate into uncorrectable patterns. This approach allows satellites to carry massive amounts of memory with a very small physical footprint, relying on mathematical redundancy rather than bulky hardware to ensure data integrity.

The emerging "sweet spot" in this frontier lies in hybrid and non-volatile technologies. By combining the speed of traditional volatile memory with the inherent radiation immunity of magnetic or resistive states, researchers are creating a new class of "instant-on" satellite memory. These hybrid designs allow a spacecraft to recover its entire system state in nanoseconds after a radiation-induced power glitch, a feat that previously required tedious manual resets from ground control. As we move toward deeper space missions, the consensus in the field suggests that

the most successful satellites will not rely on a single "perfect" memory type, but rather a tiered architecture: ultra-hardened cells for critical logic, fault-aware DRAM for bulk storage, and non-volatile snapshots for disaster recovery.

7. Future Research Directions: The Next Horizon in Space Computing

As we look toward the next decade of satellite exploration, three major research fronts are emerging that will redefine radiation resilience beyond the current silicon-based paradigms:

1. **AI-Driven Self-Healing**

Layouts: Future memory controllers are expected to integrate lightweight machine-learning algorithms that can predict "hot spots" of radiation damage in real-time. By analyzing error patterns, the memory could dynamically remap its own internal architecture, moving critical data away from degraded sectors before a permanent fault occurs.

2. **Post-Silicon Material**

Integration: The limitations of traditional CMOS are becoming clear as we scale below 5nm. Future research is heavily focused on integrating carbon nanotubes and wide-bandgap materials like Gallium Nitride directly onto memory backplanes. These materials are chemically and physically more "indifferent" to ionizing radiation, potentially offering a path to extreme resilience without the massive area penalties of current 20-transistor designs.

3. **Quantum-Resilient Architectures:** As quantum computing begins to influence satellite encryption and communication, the underlying memory must also become resilient to the unique decoherence effects caused by high-energy cosmic rays. This represents an entirely new field of "fault-awareness" where the goal is to protect the quantum state itself from the chaotic environment of deep space.

8. Conclusion

The rapid shift toward high-performance satellite computing has fundamentally altered the landscape of aerospace microelectronics. This review has demonstrated that while

standard 6T-SRAM and 1T-1C DRAM are the engines of modern data processing, they remain critically vulnerable to the unique rigours of the orbital environment. As we have seen throughout this analysis, the transition from legacy, radiation-hardened-by-process (RHBP) hardware to high-density COTS-based architectures is not merely an option but a necessity for the "New Space" era. However, this transition requires a sophisticated, fault-aware design philosophy that moves beyond simple redundancy to embrace intelligent, circuit-level and system-level resilience.

The synthesis of the 20 seminal research works discussed in this paper reveals a clear path forward. Advanced Radiation Hardening by Design (RHBD) techniques, such as the RHRSE-20T and EWS-16T SRAM cells, have proven that near-absolute immunity to Single Event Upsets (SEU) and Multiple-Node Upsets (MNU) is achievable through multi-node interlocking and symmetric feedback. Simultaneously, the development of Variation-Aware DRAM (VAR-DRAM) and Selective Triple Modular Redundancy (TMR) highlights a shift toward energy-efficient reliability, where hardware is protected based on the criticality of the data it holds rather than a one-size-fits-all approach.

Looking toward the next decade of deep-space exploration and mega-constellation deployment, the "Resilience-Density Frontier" will likely be redefined by emerging materials and non-volatile technologies. The inherent radiation immunity of Carbon Nanotubes and the "instant-on" recovery capabilities of NV-SRAM hybrids offer a glimpse into a future where the distinction between working memory and long-term storage begins to blur. By combining these material-level breakthroughs with AI-driven, self-healing layouts, satellite designers can finally bridge the gap between commercial speed and aerospace-grade durability.

Ultimately, the success of future missions from Earth-monitoring swarms to interplanetary probes depends on our ability to engineer memory that "never forgets" in an environment

that constantly attempts to erase it. This review concludes that a multi-layered defense strategy, which harmonizes ultra-hardened bit-cells with intelligent software scrubbing and robust error-correction protocols, is the most viable

framework for ensuring the longevity and success of next-generation satellite systems.

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